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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,949	05/01/2001	Chang Bae Yoon	A34174	4667
21003	7590 11/17/2004		EXAM	INER
BAKER &		MEW, KEVIN D		
30 ROCKEFELLER PLAZA NEW YORK, NY 10112			ART UNIT	PAPER NUMBER
			2664	
			DATE MAILED: 11/17/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)		
Office Antique Commence	09/846,949	YOON, CHANG BAE		
Office Action Summary	Examiner	Art Unit		
	Kevin Mew	2664		
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet wi	th the correspondence address		
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period vortice to reply within the set or extended period for reply will, by statute, any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a re within the statutory minimum of thirt will apply and will expire SIX (6) MON cause the application to become AB	eply be timely filed y (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).		
Status				
Responsive to communication(s) filed on <u>01 May 2001</u> .      This action is <b>FINAL</b> . 2b)⊠ This action is non-final.      Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims				
4) ⊠ Claim(s) 1-4 is/are pending in the application.  4a) Of the above claim(s) is/are withdray  5) □ Claim(s) is/are allowed.  6) ⊠ Claim(s) 1-4 is/are rejected.  7) □ Claim(s) is/are objected to.  8) □ Claim(s) are subject to restriction and/o				
Application Papers				
9) The specification is objected to by the Examine 10) The drawing(s) filed on 01 May 2001 is/are: a) Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex	☐ accepted or b)☐ object drawing(s) be held in abeyar ion is required if the drawing	ce. See 37 CFR 1.85(a). (s) is objected to. See 37 CFR 1.121(d).		
Priority under 35 U.S.C. § 119				
12) △ Acknowledgment is made of a claim for foreign a) △ All b) ☐ Some * c) ☐ None of:  1. △ Certified copies of the priority document:  2. ☐ Certified copies of the priority document:  3. ☐ Copies of the certified copies of the priority application from the International Bureau	s have been received. s have been received in A rity documents have been	pplication No		
* See the attached detailed Office action for a list	of the certified copies not	received.		
Attachment(s)	" <b>.</b>			
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.</li> </ol>	Paper No(s	ummary (PTO-413) )/Mail Date formal Patent Application (PTO-152) 		

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#### Detailed Action

#### **Drawings**

1. Figure 1 and Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Carlsson (US Publication 2001/0036188).

Regarding claim 1, a UTOPIA level interface in an ATM multiplexing/demultiplexing assembly (multi-service circuit that includes a ATM multiplexer/demultiplexier core that supports both Utopia level 1 and level 2 interfaces, see page 8, paragraph 0141, lines 1-9 and

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elements 20, 60, Fig. 1) in a base transceiver station interface subsystem in an IMT-2000 radio network controller, the ATM multiplexing/demultiplexing assembly including a UTOPIA level 2 execution unit (multiplexer) (ATM multiplexer/demultiplexer core, see page 3, paragraph 0054, lines 1-1-11 and element 60, Fig. 1) for supporting UTOPIA level 2 (ATM core supporting Modem/Transceiver interface and services interface, which are both Utopia 2 level interfaces, see Utopia interfaces 62 and 64, Fig. 1), and executing an ATM layer function and a UTOPIA level 1 execution unit (processor) (CPU, see element 40, Fig. 3) for performing the ATM layer function (central processing unit CPU, see element 40, Fig. 1) and supporting UTOPIA level 1 (Utopia level 1 mode for Utopia interface 34 is configured by CPU at startup, see page 8, paragraph 0141, lines 1-9), the UTOPIA level interface comprising a UTOPIA interface controller (multi-service circuit, see element 20, Fig. 1) for carrying out an ATM physical layer function to interface the layers of the multiplexer (ATM multiplexer/demultiplexer core, see page 3, paragraph 0054, lines 1-11 and element 60, Fig. 1) and the processor with each other (multi-service circuit distributes ATM cells to and from CPU via interface 34, see page 2, paragraph 0046, lines 1-8) and for performing level interface between the UTOPIA level 1 and UTOPIA level 2 (multi-service circuit couples Utopia level 1 interface 34 and Utopia level 2 interface 62, see page 8, paragraph 0141, lines 1-9, page 2, paragraph 0046, lines 1-8, page 3, paragraph 0049, lines -12, and Fig. 1) to provide a 16-bit data path (it is inherent that UTOPIA level 2 interface allows transmission and reception of 16-bit data).

Regarding claim 2, the UTOPIA level interface in an ATM multiplexing/demultiplexing assembly as claimed in claim 1, wherein the UTOPIA interface controller (multi-service circuit,

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see element 20, Fig. 1) includes transmission and reception FIFOs for temporarily storing data to be transmitted/received (ATM data are temporarily stored in two cells-deep FIFO in the upstream and downstream directions, see page 8, paragraph 0144, lines 1-8) between the multiplexer (multiplexer of the ATM core, see Fig. 2) and the processor (CPU, see element 60, 40, Fig. 2), and a UTOPIA level conversion/control unit (ATM core) for transmitting/receiving a UTOPIA level 2 control signal to/from the multiplexer (multiplexer of the ATM core) to allow the 16-bit data to be transmitted between the multiplexer and the transmission and reception FIFOs (Utopia level 2 interface 62 carries Transmit Data and Receive Data signals to allow data to be transmitted and received between the multiplexer of the ATM core and the two-cells deep transmission and reception FIFOs, see page 8, paragraph 0141, lines 6-9 and Fig. 2 and page 11, Table 2) and for transmitting/receiving a UTOPIA level 1 control signal to/from the processor to allow the 16-bit data to be transmitted between the processor and the transmission and reception F1FOs (Utopia level 1 interface 34 carries the Transmit Data and Receive Data signals to allow data to be transmitted and received between the CPU and two cells-deep transmission and reception FIFOs in the ATM core, see page 8, paragraph 0141, lines 6-9, and page 8, paragraph 0144, lines 1-8, and page 11, Table 5 and Fig. 2).

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## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carlsson in view of Rich (USP 5,784,370).

Regarding claims 3 & 4, the UTOPIA level interface in an ATM multiplexing/demultiplexing assembly as claimed in claim 2 discloses all the aspects of the claimed rejection set forth in the rejection of claim 2 above. Carlsson further discloses that each of the transmission FIFO and reception FIFO includes a two cells-deep F1FO (page 8, paragraph 0144, lines 1-8). Carlsson does not explicitly show the FIFO is 16-bit. However, Rich discloses a Utopia interface that carries data between ATM layer and physical layer and is operating in the 16-bit mode operation, and the FIFOs for storing transmission and reception data is 16 bits wide (see col. 6, lines 47-62 and col. 18, lines 16-41 and Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the FIFO structure of Carlsson such that the two cells-deep FIFO becomes two FIFOs each FIFO being 16-bit wide such as the 16-bit wide FIFO in the Utopia interface taught by Rich. The motivation to do so is to allow the size of FIFO to accommodate to the 16-bit data transfer scheme of Utopia level 2 when transmitting and receiving data to and from the Utopia interface through the transmission and reception FIFOs of the ATM core.

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Conclusion

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4. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure with respect to Utopia level interface in ATM multiplexing/demultiplexing assembly.

US Patent 6,256,308 to Carlsson

US Publication 2002/0097735 to Kosonen et al.

5. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin Mew whose telephone number is 703-305-5300. The

examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

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system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KDM

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